

Quarterly report
Chronic Microelectrode Recording Array
NIH/NINDS
Period 07/01/05 – 09/30/05

Project: NIH/NINDS **Contract-No.** HHSN265200423621C

Date: 07/01/05-09/30/05

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I. Executive summary

The overall goal of the contract No. NIH/NINDS HHSN265200423621C is to develop and test (in-vivo) a chronically implantable neural recording array and provide the device to the neuroscience community upon completion of the initial technical development phase for experimental use and evaluation.

The objective of the fourth quarter (Q4) as proposed was to:

- a) Continue to work on biocompatible coating modifications and continue fabricating UEA test chips;
- b) Finish re-routing layer mask for UEA, process development and fabrication of UEA chips (test + fully functional) with rerouting metallization
- c) Complete bench testing of the first version signal processor chip and initiate design of second version signal processor chip
- d) Fabrication of PI/BCB based coils with Au traces
- e) Design and fabricate initial spacer (UEA to coil) and preparation of SMD and flip-chip assembly
- f) Continue leakage current, impedance spectroscopy, adhesion and dissolution long term tests of SiC and Parylene encapsulation in buffer solution and subsequent further development of Parylene and SiC coating processes, materials characterization (material composition, electrical and chemical properties)
- g) Further invention disclosures and patent research

Throughout the fourth quarter, all the above mentioned objectives were accomplished.

Furthermore, the results accomplished over the past 12 months were presented at the NIH workshop in Bethesda as well as the American Academy of Nanomedicine annual meeting. Negotiations with Cyberkinetics Inc. (CKI) were initiated to establish a commercialization path and regulate the exchange of information and materials between the University of Utah and CKI.

A patent search was initiated to review the current intellectual property (IP) situation in the field of neuroprosthetic devices for central and peripheral nervous system applications worldwide. The goal is to benchmark and compare the IP generated at the University of Utah with competitors and to define niches for the placement of further patents.

II. Activity Summary

Key results for project period (Q 4) (work packages)

- Fabrication of UEA test and hot chips: fabrication of UEAs was continued. The fabrication process for the rerouting metallization was developed. UEAs with rerouting plane were fabricated. Work was commenced on optimizing fabrication processes and implementing wafer scale processes: initial etch tests on wafer sections of UEAs were performed. Furthermore, the final design for the re-routing layer on the UEA was approved.
- Development and fabrication of electronics and communications module: bench testing of all IC components (amplifiers, A/D converters, RF module, power recovery module, etc.) was completed. The 2nd version signal processor was designed and simulated.
- Development and fabrication of PI/ferrite coil: coils with final design were fabricated and assembled (bonding of two coil layers to ferrite substrate).
- Flip-chip bonding and assembly: analysis of 1st level flip chip bond between UEA and IC and final selection of SMD components for 2nd level flip chip interconnect.
- Hermetic encapsulation and layer coating: continued fabrication of test structures and deposition of silicon carbide and parylene layers on test structures. Preparation of structures and devices for biocompatibility (histology tests) in collaboration with the Keck Center for tissue engineering (Dr. P. Tresco). Layer composition and electrical properties show outstanding long term characteristics (leakage currents, impedance spectroscopy, dissolution, adhesion).

Meetings/presentations during project period (Q 4)

- Attended the NIH/NINDS workshop in Bethesda, MD
- Telephone conferences with IBMT and IZM
- Individual weekly project meetings of the project teams at the University of Utah as well as the subcontractors; meeting minutes are created in common format by all partners.

Patents (Q 4)

- Further processing of previously submitted invention disclosures. Initiation of patent search on neuroprosthetic devices to identify the profile for further invention disclosures, e.g. for the signal processor and coil design.

Organizational accomplishments (Q 4)

- Employment and training of MBA student for patenting and tech transfer support (paid through UofU Technology Commercialization Office)
- The graduate student who was hospitalized has returned and reassumed his duties
- A post-doctoral research fellow was recruited for further support
- Initiation of electrical and biocompatibility tests on PTFE based thin film layers provided by Phone conference with GBD corporation, Cambridge, MA (phone conferences and Emails)

III. Research Results and Discussion

III.a. Probe system fabrication

III.a.1 Task 1 Fabrication of ultra thin Utah Electrode Array

Description/Rationale

UEA's with the new dimensions of 7880 μ m x 7530 μ m have been fabricated. Dummy wafers with the new metallization were fabricated and sent to IZM for testing the soldering process of SMD components.

Experimental Results

Array Fabrication A 3" P type silicon wafer was diced conferring to the dimensions of the array design. The original dicing process was carried out on 1" square samples. The new process has been modified to

allow dicing of entire 3" wafers saving time and improving process uniformity. The SEM picture (Figure 1) shows fabricated UEA with new dimensions. The fins on the perimeter are removed during separation.

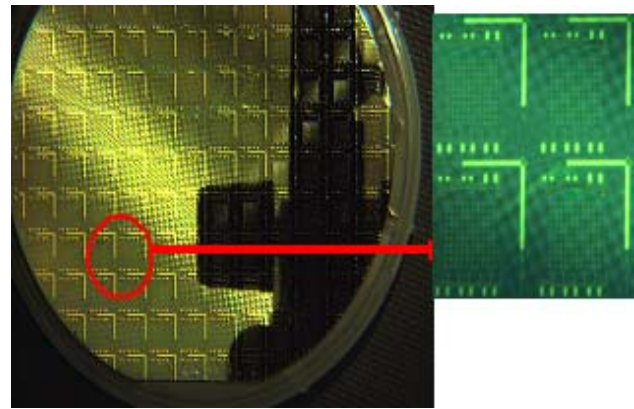
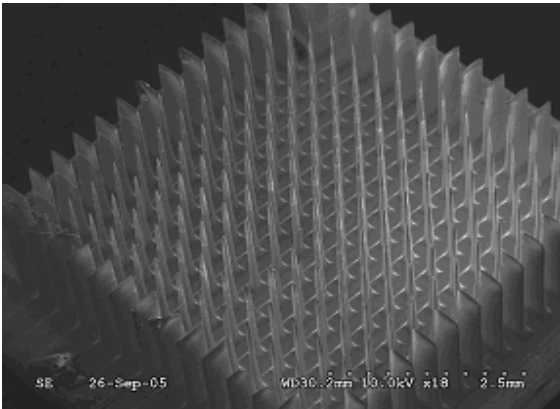


Figure 1: SEM of the new arrays with dimensions

Figure 2: Dummy wafers with the new metallization layout

Back side metallization Dummy wafers with the new metallization layer have been fabricated (Fig. 2). The back side metallization consists of a 5 metal layer stack (Pt, TiW, Pt, Au, TiW). The developed process was carried out on 4" wafers. These wafers were sent to IZM for flip chip bonding tests.

Future Plans for Next Two (2) Quarters

Results of the soldering test on dummy wafers will be used to define final changes in the metallization process. In future batches, the metallization of UEAs will be performed using the improved process prior to bump deposition and bonding of components at IZM. Further development of wafer scale processes for array fabrication (glass deposition, polishing and etching) will be carried out.

III.a.2 Task 2: Development and fabrication of electronics and communications module

Description/Rationale

The electronics/communication module will be a single CMOS integrated circuit mounted on the back of the microelectrode array. Three surface-mount capacitors mounted near the chip to provide capacitance values not achievable on chip are planned. The electronics module will amplify and process neural signals, transmit this data out of the body on an RF carrier, and receive power and command data from the power coil via a transcutaneous magnetic link.

Experimental Results

We received 40 fabricated copies of our first integrated circuit: Integrated Neural Interface chip version 1.0 (INI1). The chip was submitted to MOSIS for fabrication in March 2005 and received in late May 2005. The chips measure 4.88 mm × 6.03 mm × 240 μm. Twelve of the returned chips were packaged in small, 52-pin ceramic packages to facility bench-top testing in Harrison's lab.

- *Power/command recovery module*: this module interfaces with the power coil and converts the unregulated ac voltage on the coil into a regulated dc voltage to power the chip at 3.3 VDC. This module also extracts command data from amplitude modulations in the power waveform. The circuit interprets each amplitude change as a 'one' or 'zero' based on the length of each pulse, and loads this binary data stream into on-chip configuration and command registers. Our current chip has 128 bits of internal configuration bits. We have measured the operation of this circuit as shown below with command data being sent over a 2.64-MHz wireless link.
- *RF transmitter for reverse telemetry*: an on-chip RF transmitter transmits the digital data from the ADC and the spike detectors (433 MHz SRD band at 330 kbit/s FSK). An optimized on-chip planar spiral inductor minimizes power consumption. This circuit has been tested using a dipole antenna 13 cm from the chip to receive the FSK signal. Results are shown below.

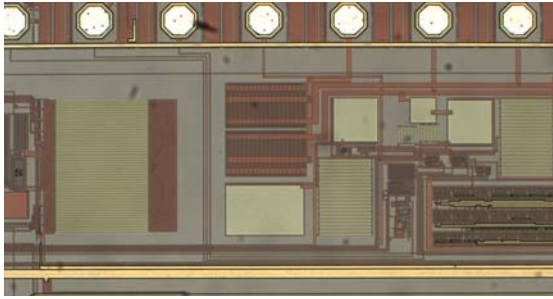


Figure 3: Photo of IN11 chip showing power recovery and forward telemetry interface circuitry. On-chip diodes rectify the ac power received by the coil, and a digital controller extracts amplitude-modulated data from the power waveform.

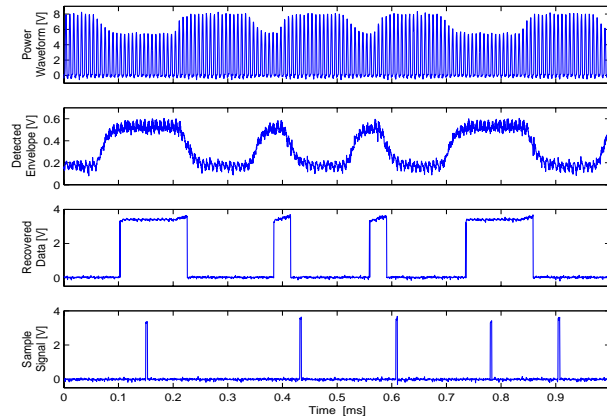


Figure 5: Operation of power/command link. From top to bottom: (a) received power waveform on the internal coil, (b) recovered envelope of the waveform, (c) digital output of the demodulation circuitry, and (d) sample signal that indicates when to shift the data signal into shift registers.

- *Neural signal amplifiers and spike detectors*: we have measured the gain (60.1 dB) and bandwidth (1.1 kHz (to block large-amplitude local field potentials) to 5.0 kHz) of the 4x4 mm² amplifier array. A comparator is used to detect spikes by comparing the output of the neural amplifier to a programmable reference level set by an on-chip digital-to-analog converter (DAC).
- *Analog-to-Digital Converter*: we have measured the linearity in the ADC (9-bit, 15 kSamples/s for neural waveforms).

To test the neural recording system (amplifiers, spike detectors, and ADC), we used an arbitrary waveform generator to play back recorded neural data from Krishna Shenoy's lab at Stanford. Fig. 5 above shows this signal amplified by our on-chip circuitry, then reconstructed from the ADC digital output. The spike detector output is shown at the bottom of Fig. 5.

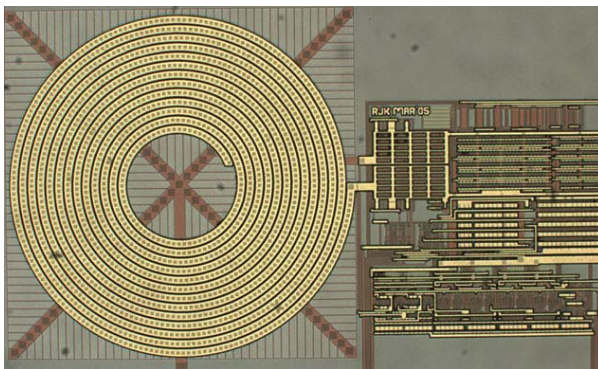


Figure 5: Photo of IN11 chip layout showing fully-integrated 433-MHz data transmitter. The on-chip planar spiral inductor measures 472 μm in diameter and acts as transmitting antenna.

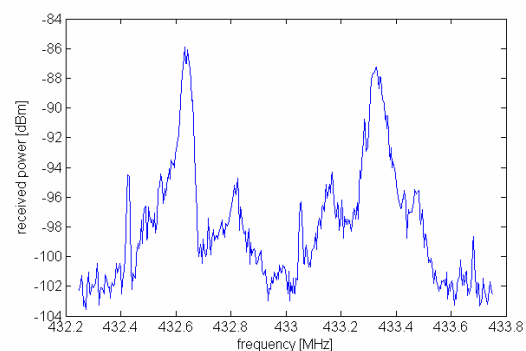


Figure 7: Spectrum of FSK data transmitter sending a typical data frame at 330 kbit/s. Dipole antenna was positioned 13 cm from chip.

Discussion/Interpretation of Results

We have completed benchtop testing of the IN11 chip. Our tests show basic functionality in all modules. Our voltage regulator successfully converts an ac voltage on a small off-chip coil into a regulated 3.3 VDC on-chip supply. The regulator requires a minimum peak coil voltage of 5.6 V for proper power

supply generation. We are currently powering the chip via a 2.64-MHz wireless link in our laboratory. Command data may be sent to the chip by amplitude-modulating the power waveform. We have sent data at a rate of 6.5 kbit/sec, although we have discovered a bug in our data receiver that leads to prohibitively high bit error rates. The source of this bug is now well understood, and this circuit will be corrected in the next version of the chip to be sent out on October 10.

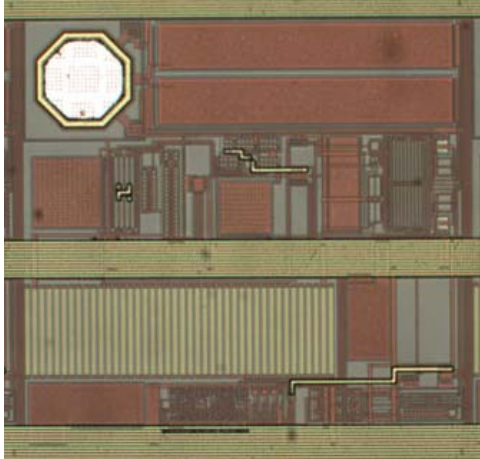


Figure 7: Photo of INI1 chip layout showing a single neural amplifier cell. The amplifier has a gain of 60 dB and a bandwidth of 1 kHz – 5 kHz. Each cell includes a spike detector for data reduction. The 70- μ m octagonal bondpad in the upper left corner contact the UEA.

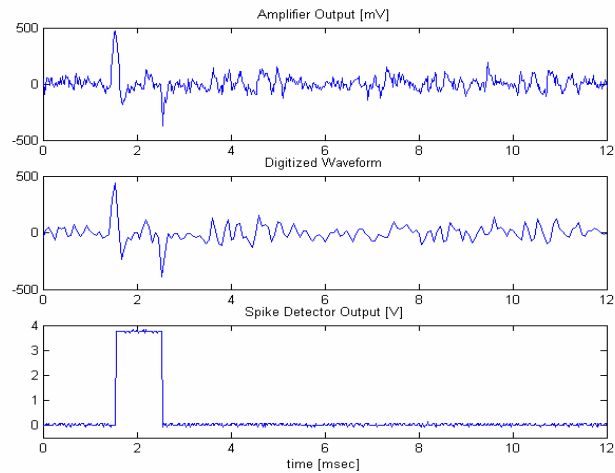


Figure 8: Response of wireless-powered chip to neural waveform played from arbitrary waveform generator. Top trace is the analog output of a neural signal amplifier. Middle trace is the waveform reconstructed from ADC output. Bottom trace is the output of the corresponding spike detector.

The neural signal amplifiers exhibit a proper gain of 60.1 dB, and a bandwidth ranging from 1 kHz to 5 kHz to isolate spikes. The input-referred noise of the amplifiers is 5.1 V_{rms} . We consider this noise level acceptable, but we aim to improve this parameter in the next design. Spike detectors function as designed, with a programmable detection threshold. The on-chip ADC works to 9-bit accuracy at a sample rate of 15 kS/s. The linearity of this circuit is excellent, with INL and DNL errors of less than ± 0.8 LSB. The 433-MHz FSK data transmitter is functional, and we have demonstrated a received signal strength of -85 dBm using a half-wave resonant dipole antenna at a distance of 15 cm while using only the on-chip 54-nH inductor as the transmitting antenna. Power consumption measurements indicate that the entire chip consumes 13.5 mW of power. The testing results are summarized in the table below.

Future Plans for Next Two Quarters

We have nearly completed design, simulation, and layout of the improved “version 2” INI2 chip. This chip will be submitted for fabrication on 10 October 2005, and will return from fabrication in late December. We are also beginning the design of RF data receiver hardware and software, and a GUI software interface to control the wireless power controller and send commands to the chip.

| Integrated Neural Interface IC Measured Performance | |
|---|--------------|
| Power/command signal frequency | 2.64 MHz |
| Minimum required receive coil voltage amplitude | 5.7 V (peak) |
| 3.3-V voltage regulator dropout ($I_L = 3$ mA) | 250 mV |
| Load regulation ($I_L = 2$ -10 mA) | 0.15 % |
| Line regulation ($V_{\text{unreg}} = 3.5$ V – 8.0 V) | <0.30 %/V |

| Integrated Neural Interface IC Measured Performance | |
|--|------------------------------|
| Maximum command input data rate (ASK) | 6.5 kbps |
| Number of Channels/Electrodes | 88 signal, 12 ground |
| Neural Signal Amplifier Gain | 60.1 dB (1.1 – 5 kHz) |
| Input Referred Noise | 5.1 μ Vrms |
| Individual Amplifier Supply Current | 12.8 μ A |
| ADC resolution (LSB = 2.4 μ V electrode referred) | 9 bits |
| ADC sampling rate | 15.0 kSamples/s |
| ADC INL/DNL error (codes 50-511) | ± 0.8 LSB/ ± 0.6 LSB |
| Spike detector threshold resolution (LSB = 4.8 μ V electrode referred) | 7 bits |
| FSK data transmission frequency | 433 MHz |
| FSK data rate | 330 kbps |
| Received signal power at distance of 13 cm | -86 dBm |
| Total chip power dissipation | 13.5 mW |
| Total chip area (0.5- μ m, 2P3M CMOS) | 27.3 mm ² |

III.a.3 Task 3: Development and fabrication of PI and BCB coils

Description/Rationale

Electrode width, winding separation and Au thickness of the coils are 15 μ m. Ni/Au metal for pads are used to interconnect coil and UEA. A Polyimide (PI) layer is used as substrate and glued to a ferrite substrate.

Experimental Results

PI coil manufacturing: the PI coils are fabricated on a 4" Si wafer. Each wafer carries 100 coils with different designs. A total of about 1000 coils will be manufactured. The process for the double layer coils consists of four plating steps, starting with the polymer layer and ending with the formation of Ni/Au interconnection pads. Figure 10 shows the optical microscope images of the electroplated Au coils with thickness of about 15 μ m.

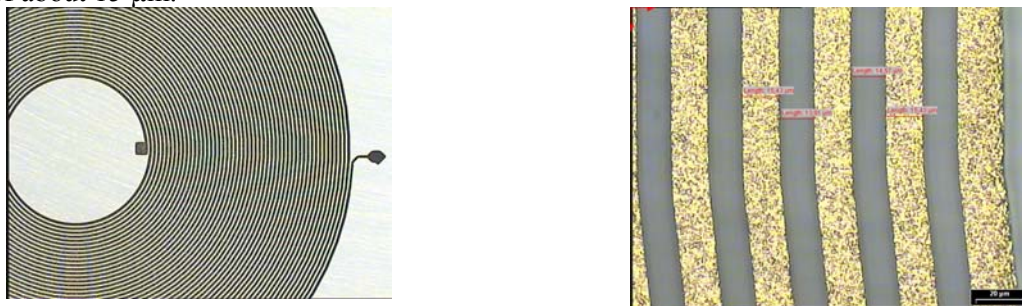


Figure 9: Optical microscope images of an electroplated Au-coil on polymer layer

BCB coil manufacturing: manufacturing of BCB coils is in progress. BCB is used as alternative to PI.

Discussion/Interpretation of Results

Based on the simulated data, the flexible coil concept was developed and manufactured. With PI and BCB two approaches for coil manufacturing are now available.

Future Plans for Next Two (2) Quarters

We plan to complete manufacturing of coils with PI and BCB. We will further develop and improve the process of mounting PI and BCB coils on the ferrite substrates. Manufactured coils will be sent to the University of Utah for electrical characterization.

III.a.4 Task 4: Flip-chip bonding and assembly

Description/Rationale

We have designed and manufactured masks for electroplating of the Au/Sn bumps. Chips have been embedded into a support wafer and the bumping process is in progress. A detailed analysis of the UEA was performed and small cracks were found on the top surface and underneath the pad metallization. Based on this result, grinding and polishing process of the UEA-wafer is changed. A SnCu0.7 (type 4) solder paste was selected. This paste will be used to assemble the SMDs. The ceramic spacers which will be placed between coils and UEAs were delivered and inspected.

Experimental Results

Au/Sn electroplating: AlN substrates with laser machined windows sufficiently large to accommodate the chips were fabricated. An adhesive film was laminated on the front side of a substrate and the chips were inserted into the recesses on the AlN substrate. The substrate is turned upside down and an epoxy is dispensed into the gaps between substrate and chips. After removing the adhesive film the embedded substrate is ready for thin film processing (see Fig. 10).

For the bumping process, a thin TiWN layer (230nm) and 200 nm Au are sputtered uniformly across the entire substrate. TiWN serves as a diffusion barrier for the Aluminum pads which are cleaned prior to deposition by back-sputtering with Argon. The sputtered Au layer is used as plating base. A positive photoresist is applied as plating mask. The sputtered Au layer acts as a electrode during electroplating. 25 μm of Au and 6 μm of Sn are electroplated. After metal deposition the photoresist is stripped and the plating base is removed by wet etching. After dicing, the epoxy is removed and the chips are ready for bumping. A substrate was laser machined and 4 chips were inserted from the rear side. The substrate is ready for photoresist processing. The alignment accuracy of the four chips will be measured after photoresist deposition. The best alignment accuracy for this process is 5 μm .

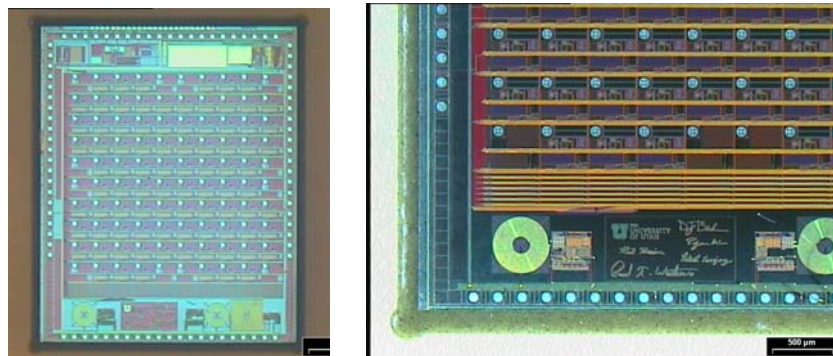


Figure 10: single chip embedded in an AlN substrate (overview and detailed picture)

Inspection of the UEA: cross sectioning was performed to investigate the interconnections between dummy IC and UEA. Cracks were observed on the surface of the UEA and some Au/Sn bonded contacts showed craters underneath the pad metallization of the array. A detailed analysis indicated that the top surface of the UEA was extremely rough. We suggested changing the grinding and polishing procedure of the top surface of UEA to get smooth surfaces with less stress. Figure 11 shows an optical microscopy image of a cross section through the UEA.

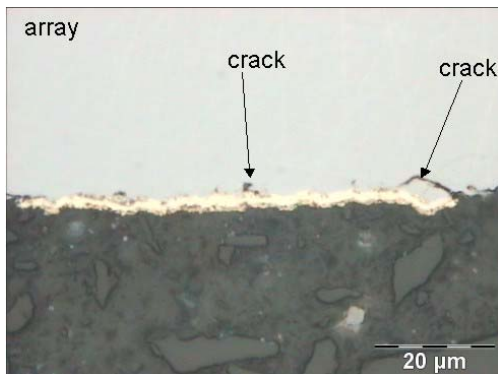


Figure 11: Optical microscopy image of a cross section of UEA; the light gray area on top is the silicon of the UEA; cracks were observed underneath the pad which could lead to further crack formation and a delamination of the pad metallization after or during Au/Sn bonding

Spacer: ceramic spacers for the interconnection between UEA and coil were delivered. Figure 12 shows optical microscopy images of spacers prior to and after reflowed SnCu0.7 solder. The reflow tests indicated good wetting of the bond pads.

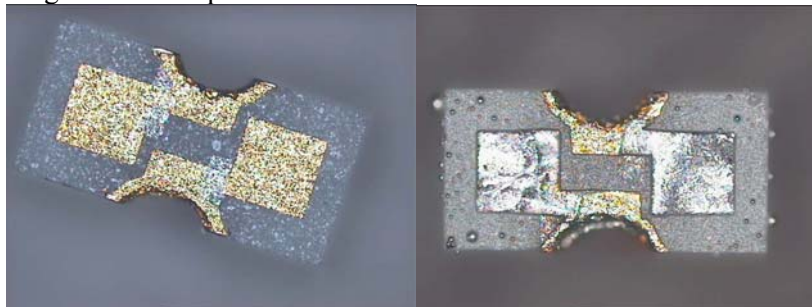


Figure 12: Top view of the ceramic spacer (left) and after SnCu0.7 solder reflow test (right)

Underfilling: Namics U8433 is selected as underfiller because of its good flow properties even in confined spaces. The compatibility of Namics U8433 to the SiC coating process was tested. The SiC is deposited at temperatures above 200 °C for 2 hours. These temperatures are quite close to the degradation temperature of the epoxy underfiller. Thermogravimetric (TGA) measurements have been performed. TGA results show only a low weight loss of 0,15 % after 2 hours at 200 °C (see Figure 13). The delamination risk was studied with underfiller and SiC coated wafers. The coated wafers have been analyzed in initial state and, as accelerated test scenario, after pressure cooker storage (121 °C, 100 % rel. humidity, 2 bar) by acoustic microscopy. No delaminations/changes could be detected until 48 hours, (neither visually nor acoustically). Investigations are still ongoing. In summary the selected underfiller material shows good compatibility to the SiC coating process with temperatures around 200 °C and can thus be used for the UEA assembly process.

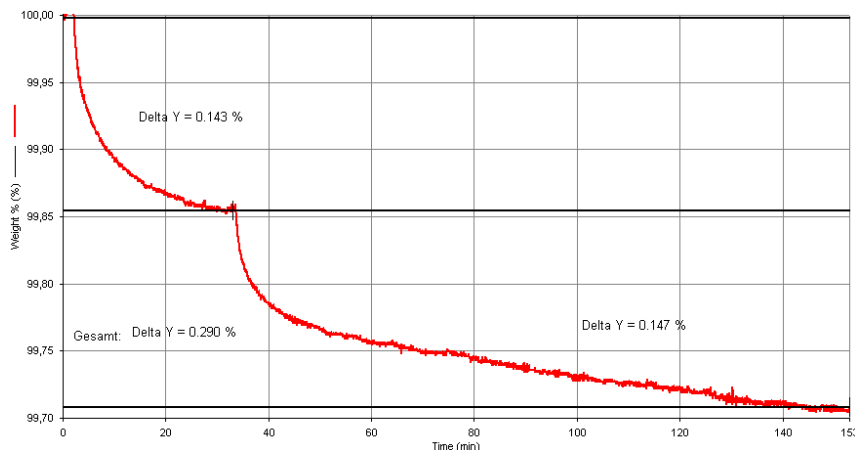


Figure 13: Thermogravimetric measurement of Namics U8433 with a test profile: 30min at 125°C, 120min at 200°C under oxygen atmosphere. Weight loss caused by humidity desorption is 0.14 %, thermal degradation effects cause a weight loss of 0.15 %.

Discussion/Interpretation of Results

The Au/Sn electroplating process for the single chip bumping is in progress. Ceramic spacers were delivered and first solder wetting tests showed good results. Tests are still ongoing to investigate the properties of the selected underfilling material.

Future Plans for Next Two (2) Quarters

The Au/Sn single chip bumping will be finished. The assembly process will be fully developed. The assembly process includes Au/Sn reflow soldering with analysis of the interconnections by cross sectioning, SMD--coil mounting with SnCu0.7 reflow, and setup for the underfilling. Finally about 10 functional sensor packages will be assembled.

III.a.5 Task 5: Hermetic encapsulation and layer coating

Description/Rationale

To investigate the encapsulation behaviour and quality of SiC and Parylene C, samples have been prepared for in vitro investigations to simulate the physiological ambience inside the body. A low deposition temperature ($< 200\text{ }^{\circ}\text{C}$) SiC process was developed to prevent damage to polymeric flip-chip underfill material. Leakage current tests, impedance spectroscopy tests, dissolution tests and adhesion tests are being performed on both SiC and parylene coatings. In order to achieve better encapsulation, parylene is coated on top of the SiC layer. The adhesion between SiC and parylene is being investigated.

III.a.5.1 SiC, Parylene Coatings - Impedance Spectroscopy & Leakage Current Tests

Experimental Setup

Four IDE structures (Figure 15) were coated with about $2.9\mu\text{m}$ thick Parylene C. Two structures were coated with $0.4\mu\text{m}$ SiC at 280°C and two structures were coated with $0.4\mu\text{m}$ thick SiC at 200°C . These structures were soldered to wires insulated by Teflon. The other ends of these wires were projected through a circular FR4 material which is glued to a bottle cap (Figure 14 and 15).

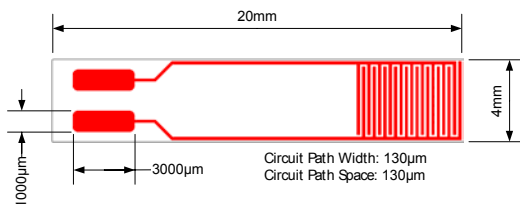


Figure 14: Dimensions of the IDE structure.

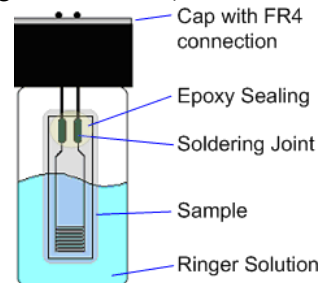


Figure 15: Design of the sample bottle.

A cap with the structure was fitted onto a bottle filled with 0.9% NaCl physiological solution. Only the IDE part of the structures was immersed in the solution and the contact pads are kept above the solution. The contact pads are encapsulated in an epoxy to prevent failure due to water vapour (Fig. 15 and 17). The bottles were maintained at 37°C . After five days the structures were investigated using impedance spectroscopy (50mV AC, Solartron 1255 Frequency Response Analyzer, Solartron 1287 Electrochemical Interface).



Figure 16: IDE structures assembled on bottle cap.



Figure 17: Test samples immersed in 0.9% NaCl solution.

Leakage current tests were performed for 20 days on each sample. The bottles were placed in a sample holder. A multiplexer box with spring mounted contact pins for electrical contact to the bottle cap is attached on the top of the holder. The multiplexer is connected to a voltage source and an ammeter to measure the leakage current. The whole system is connected to a PC for current recording and multiplexer control (Figure 18). Each contact is coupled with a 10^3 Ohm resistance to produce a defined value when a sample has lost its encapsulation. Due to this resistance, if the measured current is about 10^{-3} A the sample will be defined as being defective.

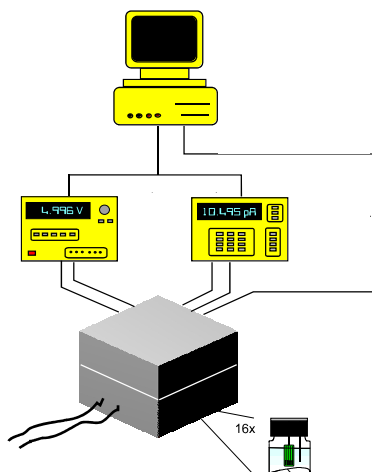
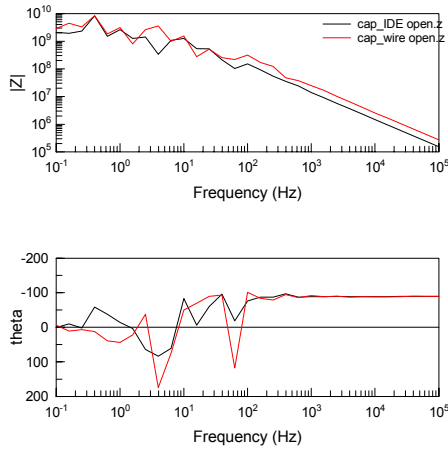


Figure 18: Schematic of the leakage current test system.

The block heater is kept at 37°C by circulating water. A voltage of 5V DC has been used to measure any leakage current between the two comb structures.

Experimental Results

The measured impedance results of unassembled wires (pre assembled bottle without test structure and solution) and unfilled IDE structures (assembled bottle without solution) show high impedance at low frequencies (Figure 20). This was done as reference to compare the results of assembled test structures. The leakage current investigation on the 280°C SiC samples showed impedances between 10^5 Ohm and 10^6 Ohm (at low frequencies). The results on the 200°C SiC samples showed an impedance of 10^5 Ohm and a very low impedance of about 10^2 Ohm (Fig. 20). Three Parylene C encapsulated structures showed an impedance of about 10^8 Ohm to 10^9 Ohm and one (3a) of about 10^4 Ohm (Fig. 21).



| | | |
|-----------|---|-----------|
| Sample 2a | → | 280°C SiC |
| Sample 2b | → | 280°C SiC |
| Sample 2c | → | 200°C SiC |
| Sample 2d | → | 200°C SiC |

| | | |
|-----------|---|------------|
| Sample 3a | → | Parylene-C |
| Sample 3b | → | Parylene-C |
| Sample 3c | → | Parylene-C |
| Sample 3d | → | Parylene-C |

Figure 19: Impedance of unassembled wire (black line), unfilled IDE structure (red line) and sample identification.

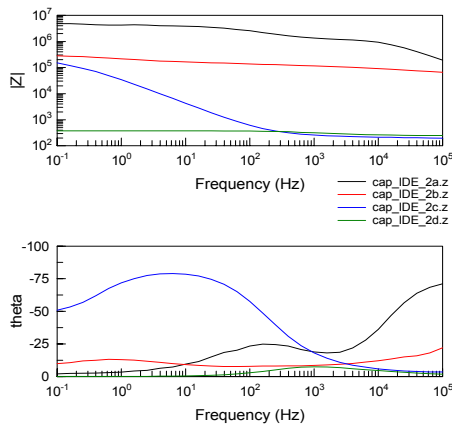


Figure 20: Impedance of SiC samples.

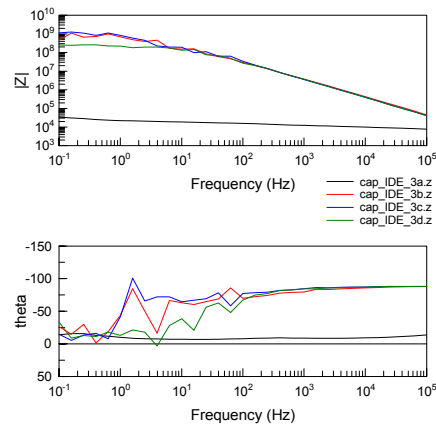


Figure 21: Impedance of Parylene-C samples.

Following the first five-day impedance test the samples were investigated for an additional 20 days in the leakage current test system and are still running. The leakage current tests on SiC coatings are in progress.

The Parylene C samples show impedances of between 10^5 Ohm (sample 3a) and 10^9 Ohm at the beginning of the leakage current test (Fig. 22). Sample 3a demonstrated an increased current on the second day of the test and quickly reached the detectable maximum (10^{-3} A). The other two samples displayed similar behavior after about 5 days (3b) and 10 days (3d). Sample 3c had almost constant low leakage current for more than twenty (20) days (impedance of about 10^9 Ohm and 10^{-9} A).

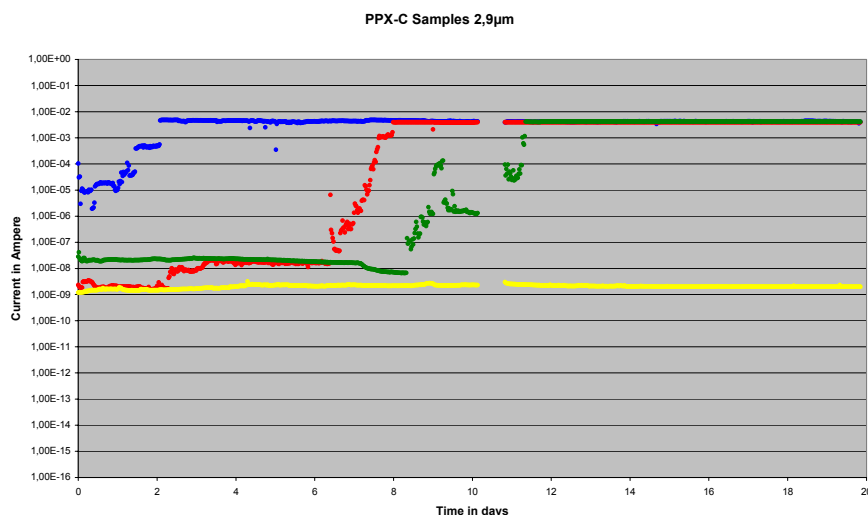


Figure 22: Leakage current measurement of Parylene C samples.

Discussion/Interpretation of Results

The initial investigation of encapsulated samples after five days in physiological solution and temperature shows promising results regarding the behaviour of SiC and Parylene C. Although the 200°C coated SiC layers show low impedance and therefore high leakage current. One 200°C SiC sample (2c) even shows an impedance of about 10^5 Ohm at 50mV AC. After placing this sample into the leakage current test system with 5 Volts DC the current was about 10^{-3} A and therefore defined as being defect.

The Parylene C coated samples show relative high impedance except one sample (3a) that showed 10^6 Ohm (10^{-6} A) in contrast to the other three with 10^9 Ohm (10^{-9} A) in the leakage current test. Besides the sample 3c the others failed after several days, which is a typical behaviour for this type of encapsulation. This could be a result of local adhesion problems or layer defects during sample preparation. The impedance of the Parylene C samples at the beginning of the test was higher than the SiC ones. This could lead to an interesting combination of both materials as encapsulates.

Future plans for the next (2) quarters

In the reported period the leakage current test system was upgraded to additional analysis modules for testing more samples. Selected software improvements will be carried out and finished in October to allow accelerated statistical analysis. SiC, Parylene C coatings will be investigated individually and combined as multilayers. Besides the leakage current behavior of both investigated materials, the coating of silicone over Parylene C and SiC encapsulates as a measure to improve handling and mechanical stability is planned.

III.a.5.2 SiC, Parylene Coatings- Dissolution & Adhesion Tests

Experimental setup and results

The SiC layer was deposited at temperatures 150° C to 275° C. High dilution, high temperature, and silane starving condition deposited films with high silicon-carbon density were fabricated (Fig. 23).

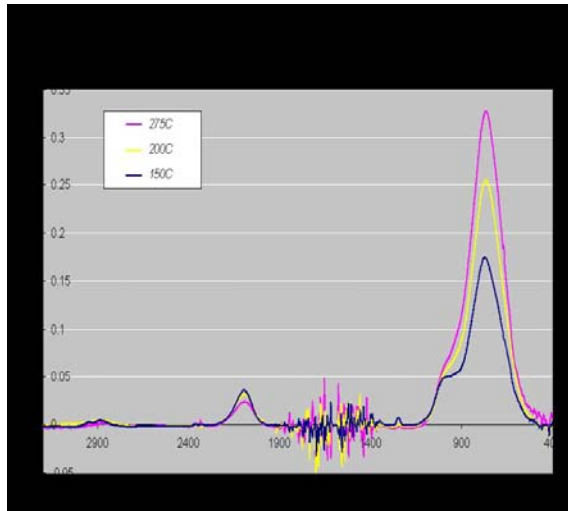


Figure 23: SiC FT-IR absorbance normalized to a thickness of 0.4 μm . At high hydrogen dilution and silane starving condition, high silicon-carbon density was obtained.

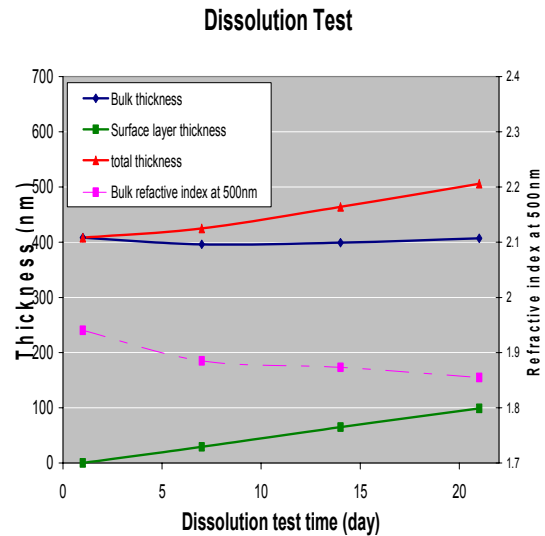


Figure 24: After 28 days in 90 °C PBS, SiC thickness increased slightly, which may be due to surface oxidation

Dissolution rate tests were performed by immersing the SiC and Parylene deposited Si samples in 90° C PBS solution and measuring the thickness of films every five (5) days. The test results in Fig. 24 show that all the SiC films increase in thickness, which may due the surface oxidation. These results suggest that SiC may provide better protection over time (self passivation). During these tests, the film with micro defects generated larger square defects (Fig. 25). This may be due to the seepage of PBS through micro cracks and etching of silicon in a preferential plane.

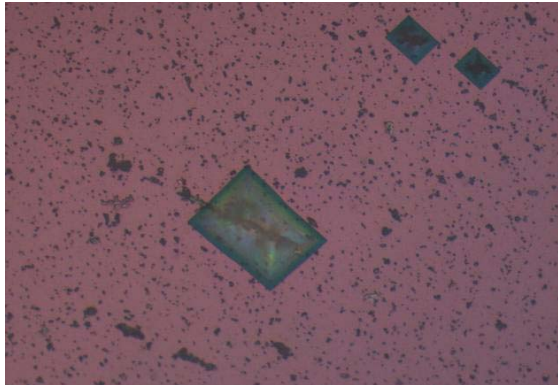


Figure 25: At encapsulation defects, PBS etches the Si wafer and form square defects



Figure 26: Parylene adheres to a-SiC:H after 1 day in 90 °C PBS

The adhesion between SiC and parylene was evaluated using the ASTM 3359A standard. For these tests, SiC was first deposited on a silicon wafer, cleaned by a plasma etch and treated with an adhesion promoter (silane A174). Parylene was deposited on these samples using standard deposition procedures. The adhesion test result show that parylene adheres well to SiC in dry test condition and even after 1 day in 90° C PBS solution (Fig. 26). The adhesion between SiC and underfiller material was evaluated by acoustic microscopy and ASTM3359A standard. Adhesion test results are shown in Fig. 27 and 28.

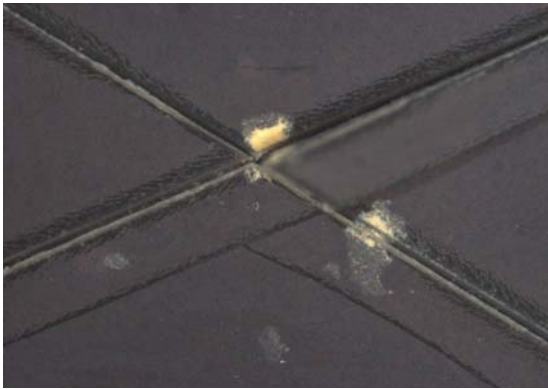


Figure 27: Without scratched underfiller, the underfiller remained on the substrate after more than 11 days in 90°C PBS.

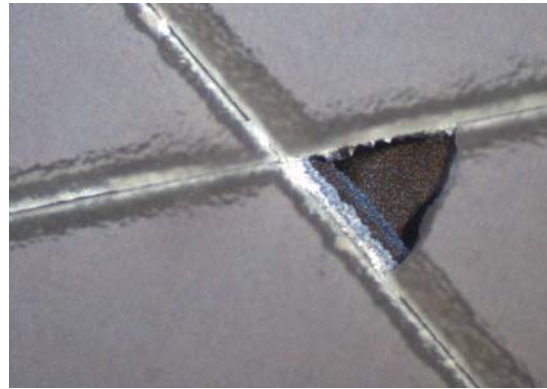


Figure 28: With scratched underfiller, the underfiller starts delaminating from substrate after 5 days in 90°C PBS.

Discussion/Interpretation of results

We have determined that lower SiC deposition temperature yields poorer adhesion. By controlling the volume of reactive and dilution gas ratio, we can control the Si-C bonding density and thereby the film porosity. High dilution, high temperature and silane starving condition allow deposition of films with high Si-C density. It was found that a higher Si-C bonding density yields a higher compressive film stress and thus poorer protection due to possibility of micro-cracks. This indicates that less dense SiC film may be better suited for encapsulation. We have also found that parylene adheres well to SiC. The adhesion between SiC and underfill material is good when the films are not scratched, i.e. provided no mechanical damage is done to the film.

III.b.1 Task 6: Testing and validation of probe systems (in-vitro/in-vivo)

n/a at this stage of the project except for definition of test program

III.b.1.1 Bench testing of interface/electronics

n/a at this stage of the project

III.b.1.2 In-vivo testing of interface

No in-vivo testing at this stage of project

IV. Concerns

During the 4th quarter of the project no major delays or deviations were observed. We would however like to inform NIH/NINDS that modifications in the flip chip process as well as the integration of external amplifier bias tuning resistors onto the signal processor chip have resulted in increased complexity for the 2nd version design of the signal processor. This may ultimately lead to a two to three week delay in the delivery of the 2nd version signal processor. Provided that testing can be accelerated, this should not lead to delays in the assembly of the complete neural interface chip prototypes, scheduled for the December 2005 / January 2006.

Salt Lake City, Utah, October 9th 2005

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